Performance Analysis and Optimization

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Instrumentation

- Application-specific (manual) instrumentation...
  - Most robust
  - Minimal overhead (omp_get_time)
  - Insensitive to sampling effects
  - Application-specific knowledge can different based on usage (e.g. different levels of MG)
  - High effort / large reward

- Auto-instrumentation (TAU, Advisor, Vtune)...
  - Minimal effort
  - Integrated visualization
  - Sampling effects can confuse performance analysis
  - Using the same function many different ways can confuse analysis
  - Can have high overhead (Advisor/Vtune)
The **Roofline Model** is a throughput-oriented performance model...

- Tracks rates not time
- Augmented with Little’s Law
  \( \text{concurrency} = \text{latency} \times \text{bandwidth} \)
- Independent of ISA and architecture
  (applies to CPUs, GPUs, Google TPUs\(^1\), etc...)

Informs developers which routines are underperforming the processor’s capabilities == which routines to optimize

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https://crd.lbl.gov/departments/computer-science/PAR/research/roofline
Use by NESAP

- NESAP is the NERSC KNL application readiness project.
- NESAP used Roofline to drive optimization and analysis on KNL
  - Bound performance expectations (ERT)
  - Use Vtune to quantify DDR and MCDRAM data movement
  - Compare KNL data movement to Haswell (sea of private/coherent L2’s vs. unified L3)
  - Understand importance of vectorization
  
Roofline for NESAP Codes

**MFDn**

- Roofline Model
- wo/FMA
- 1 RHS
- 4 RHS
- 8 RHS

**EMGeo**

- Roofline Model
- wo/FMA
- Original
- SELL
- SB
- SELL+SB
- nRHS+SELL+SB

**PICSAR**

- Roofline Model
- wo/FMA
- Original
- w/Tiling
- w/Tiling+Vect

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GFLOP/s

Arithmetic Intensity (FLOP/byte)
Intel Advisor

Intel Advisor is a performance analysis tool (evolved from vector advisor)

Background

- https://www.youtube.com/watch?v=h2QEM1HpFgg

Running Advisor on NERSC Systems

<table>
<thead>
<tr>
<th>Line</th>
<th>Source</th>
<th>Total Time</th>
<th>%</th>
<th>Loop/Function Time</th>
<th>%</th>
<th>Traits</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>#pragma omp parallel for</td>
<td>9.890s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>for(k=1;k&lt;dim+1;k++)</td>
<td>102.403s</td>
<td>100</td>
<td>157.994s</td>
<td>150</td>
<td>FMA</td>
</tr>
<tr>
<td>27</td>
<td>for(j=1;j&lt;dim+1;j++)</td>
<td>102.403s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>#pragma novector</td>
<td>102.403s</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>for(i=1;i&lt;dim+1;i++){</td>
<td>102.403s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>int ijk = i<em>iStride + j</em>jStride + k*kStride;</td>
<td>53.651s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>new[ijk] = -6.0*old[ijk]</td>
<td>53.651s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>+ old[ijk*1Stride]</td>
<td>53.651s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
[loop in bench_stencil_ver4$omp$parallel_for@193 at stencil_v2.c:193]
Total Performance: 18.98 GFLOPS
Total L1 Arithmetic Intensity: 0.41 FLOP/Byte
Self Elapsed Time: 0.000 s
Total Elapsed Time: 9.956 s

File: stencil_v2.c:193 bench_stencil_ver4$omp$parallel_for@193

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<th>Traits</th>
</tr>
</thead>
<tbody>
<tr>
<td>191</td>
<td><code>Startime = omp_get_wtime();</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>192</td>
<td><code>while(ElapsedTime &lt; TIME){</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>193</td>
<td><code>#pragma omp parallel for schedule(static,1)</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>194</td>
<td><code>for(tile=0;tile&lt;Tiles*Tiles;tile++)</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Selected (Total Time): 8.004 ms
likwid

- **likwid**
  - Performance counter infrastructure for x86
  - No sampling (simply reads counters)
  - <1% overhead (SDE/VTune/Advisor see >10x)
  - **MPI Scalable** (can run across many processes)
  - Useful for high-level characterization (not connected to source)

- **Now runs on NERSC machines:**
  - Verified on Haswell
  - Needs Vtune and likwid modules
  - `#SBATCH --perf=vtune`
  - Likwid-perfctr
  - Used to characterize AMReX ECP apps…

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**AMReX Application Characterization**

(2Px16c HSW == Cori Phase 1)

- L2
- L3
- DRAM
- Roofline

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**Bandwidth (GB/s)**

- 8
- 16
- 32
- 64
- 128
- 256
- 512
- 1024

- HPGMG (32Px1T)
- HPGMG (4Px8T)
- Combustor (32Px1T)
- Combustor (4Px8T)
- MFIX (32Px1T)
- Nyx (32Px1T)
- Nyx (4Px8T)
- PeleLM (32Px1T)
- WarpX (32Px1T)
- WarpX (4Px8T)
Threading vs. Processes

- Threads provide no inherent compute advantage over processes
- Threads incur additional overhead (omp parallel, single, barrier, …) == slower in the perfectly parallel world
- Threads provide easy access to shared memory…
  - Some codes are easier to parallelize with threads than MPI
  - Easier to avoid data duplication (memory requirements) with threads than processes
  - Threads can access shared data in cache rather than copying data between processes
  - Using threads simplifies topology-aware MPI process mapping (MPICH_RANK_REORDER is often insufficient)… topology-aware is still important on Aries/Dragonfly and IB/FatTrees
  - Using threads provides on-ramp to GPUs and other emerging architectures
**Threading Experiments/Analysis**

- **Fix process concurrency, increase threading ...**
  - Ideally, function runtime should scales as $O(1/\text{omp\_num\_threads})$
  - Identify functions that plateau (saturation)
  - Identify functions that are flat (sequential bottlenecks)
  - Identify functions that increase (duplicated work... e.g. use of Fortran’s sum(a(:)) )

- **Fix hardware concurrency (cores), increase threads while reducing processes.... (32x1, 16x2, 8x4, 4x8, 2x16, 1x32)....**
  - Distinguish true flat MPI (no –fopenmp) from hybrid w/1 thread (-fopenmp + OMP\_NUM\_THREADS=1) == threading overhead
  - Identify functions that are flat, better with threads, or better with processes
  - Especially useful for communication routines
KNL-specific issues

- GNU and Intel runtimes treat OMP_PLACES/PROC_BIND differently...
  - use same compiler for all threaded routines / know which settings to use
  - (I use KMP_AFFINITY with Intel)

- If you can fit in 16GB, run in quadflat...
  - avoids cache aliasing issues where some nodes are slower than others
  - Can manifest as abnormally high MPI_Wait times and degraded scalability
  - Use srun … numactl –m1 ./a.out … (or use –p1 or no numactl but allocate key data in HBM)

- use large contiguous blocks with 2M pages for data and MPI buffers...
  - Better performance for complex (less streaming) memory access patterns
  - minimizes NIC TLB pressure == higher MPI bandwidth

- Examine vectorization reports...
  - KNL is very slow if not vectorized
Questions